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Attorney's Docket No.: 10417-084001 / F51-134741M/KIK

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Izuo Iida
Serial No. : 09/876,554
Filed : June 7, 2001
Art Unit : Unknown
Examiner : Unknown
Title : METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE

Attention: Official Draftsman
Commissioner for Patents
Washington, D.C. 20231

TRANSMITTAL OF FORMAL DRAWINGS

Please substitute the enclosed 12 sheets of formal drawings for the corresponding drawings presently in the application.

Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: June 18, 2001

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Rose Papetti
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FIG.1

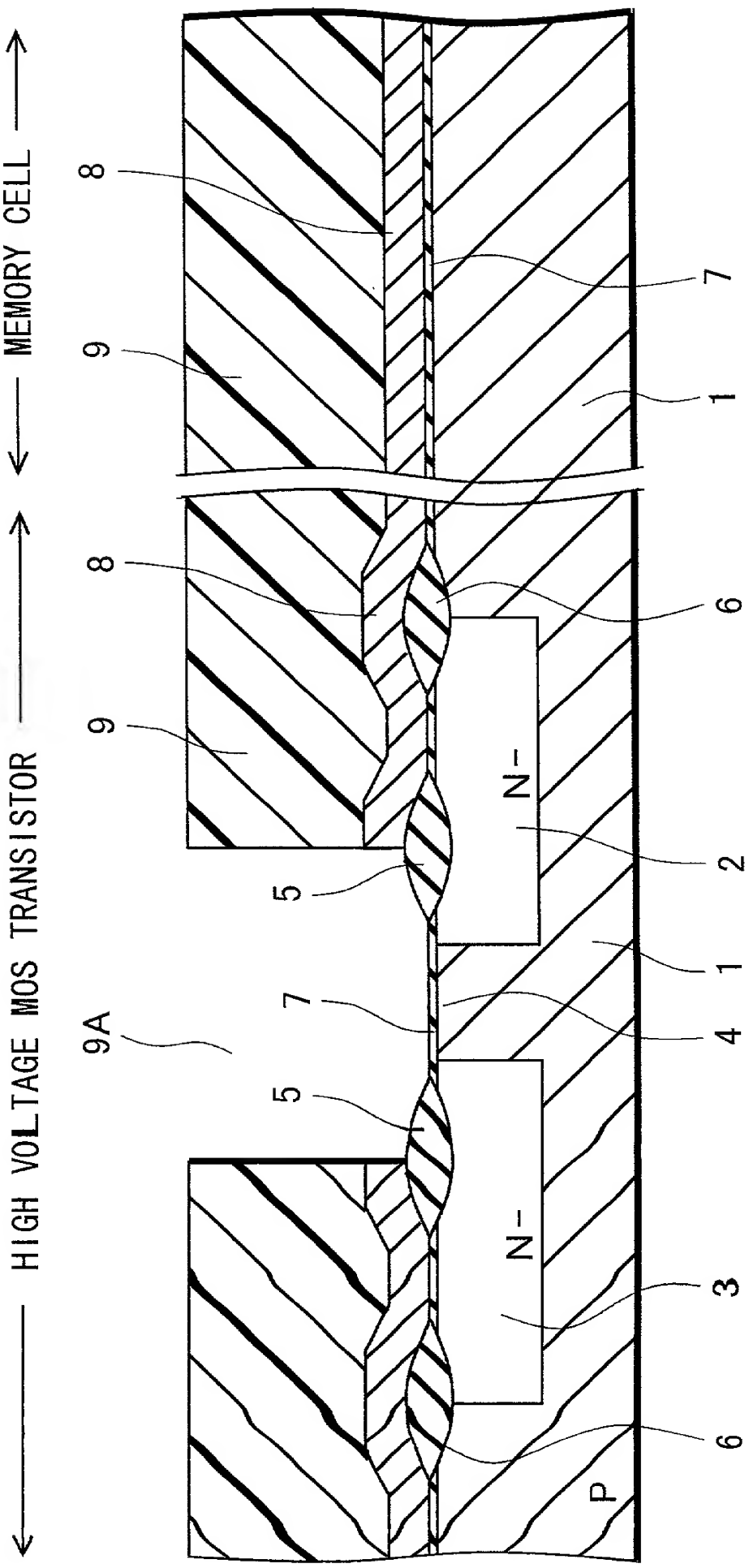
HIGH VOLTAGE MOS TRANSISTOR
MEMORY CELL
8
9
8
9
9A
5
7
5
N-
N-
7
1
6
2
1
4
3
6
P

FIG.2

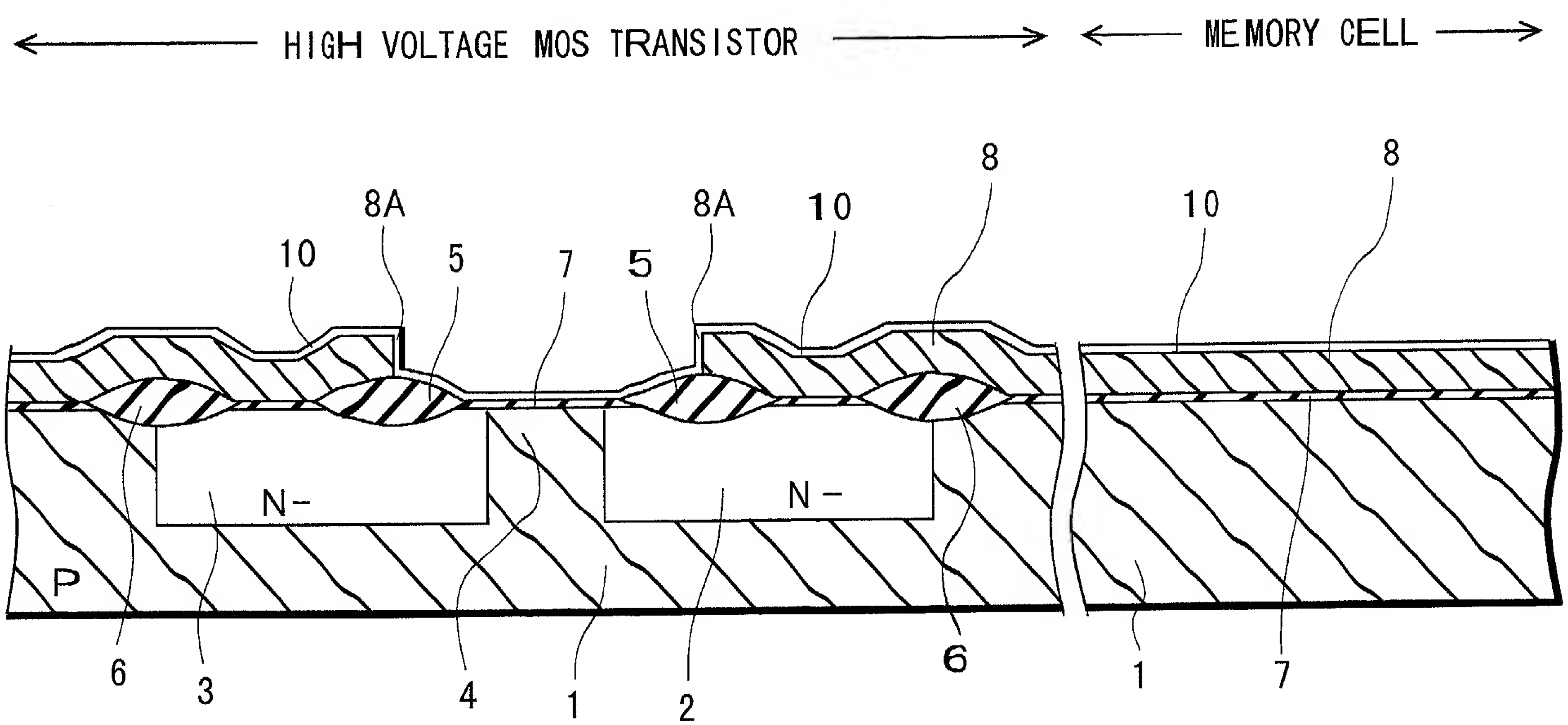
HIGH VOLTAGE MOS TRANSISTOR
MEMORY CELL
8A
10
5
7
5
8A
10
8
10
8
N-
N-
P
6
3
4
1
2
6
1
7

FIG.3

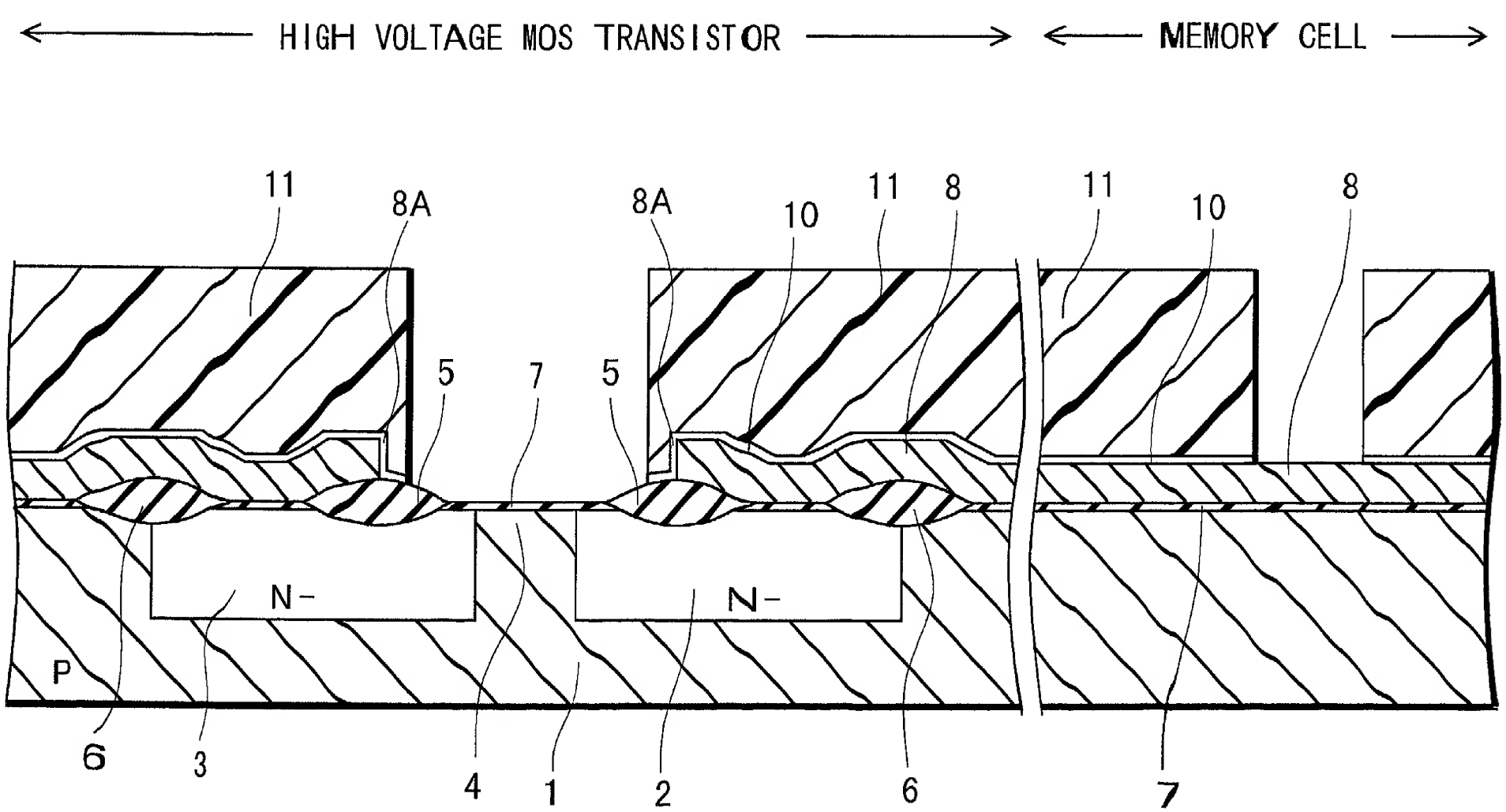
HIGH VOLTAGE MOS TRANSISTOR
MEMORY CELL
11
8A
5
7
8A
10
11
8
11
10
8
N-
N-
P
6
3
4
1
2
6
7

FIG.4

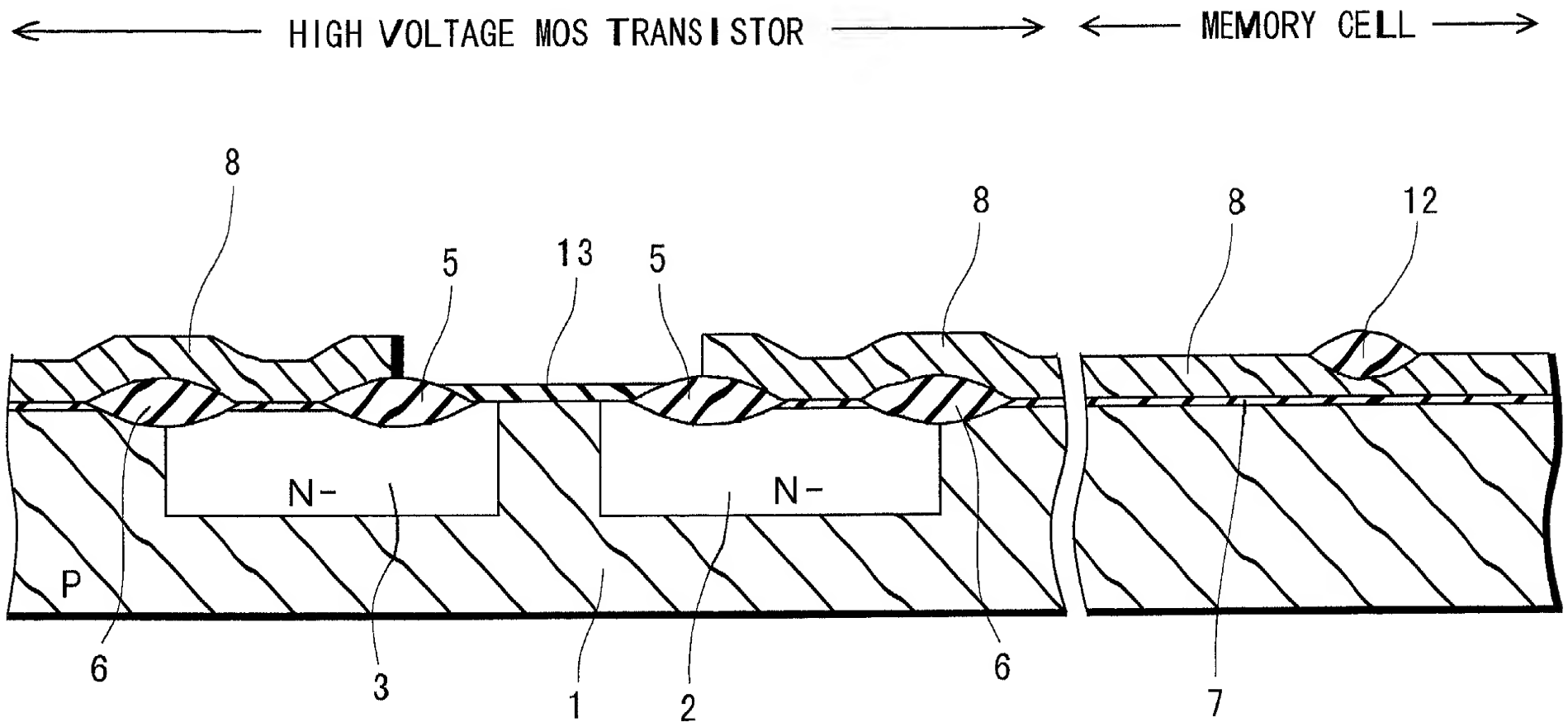
HIGH VOLTAGE MOS TRANSISTOR
MEMORY CELL
8
5
13
5
8
8
12
N-
N-
P
6
3
1
2
6
7

FIG.5

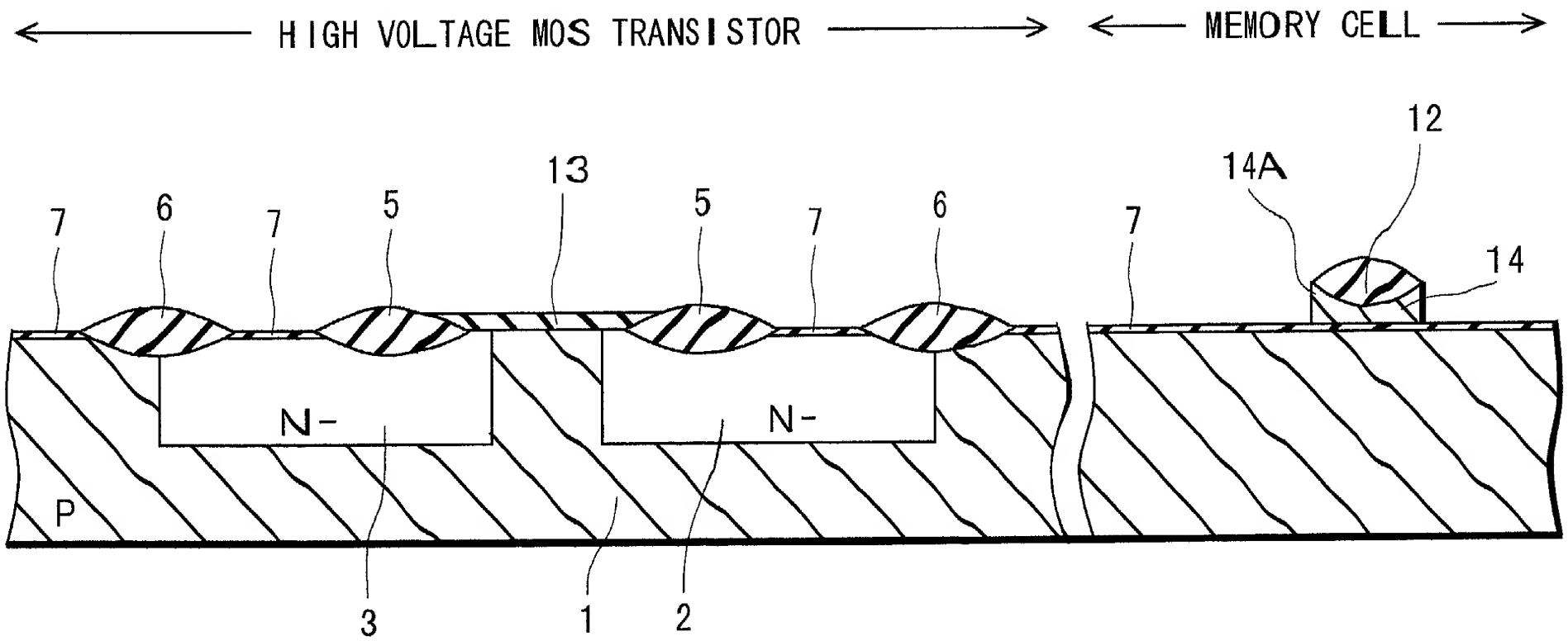
HIGH VOLTAGE MOS TRANSISTOR
MEMORY CELL
7
6
7
5
13
5
7
6
7
14A
12
14
N-
N-
P
3
1
2

FIG.6

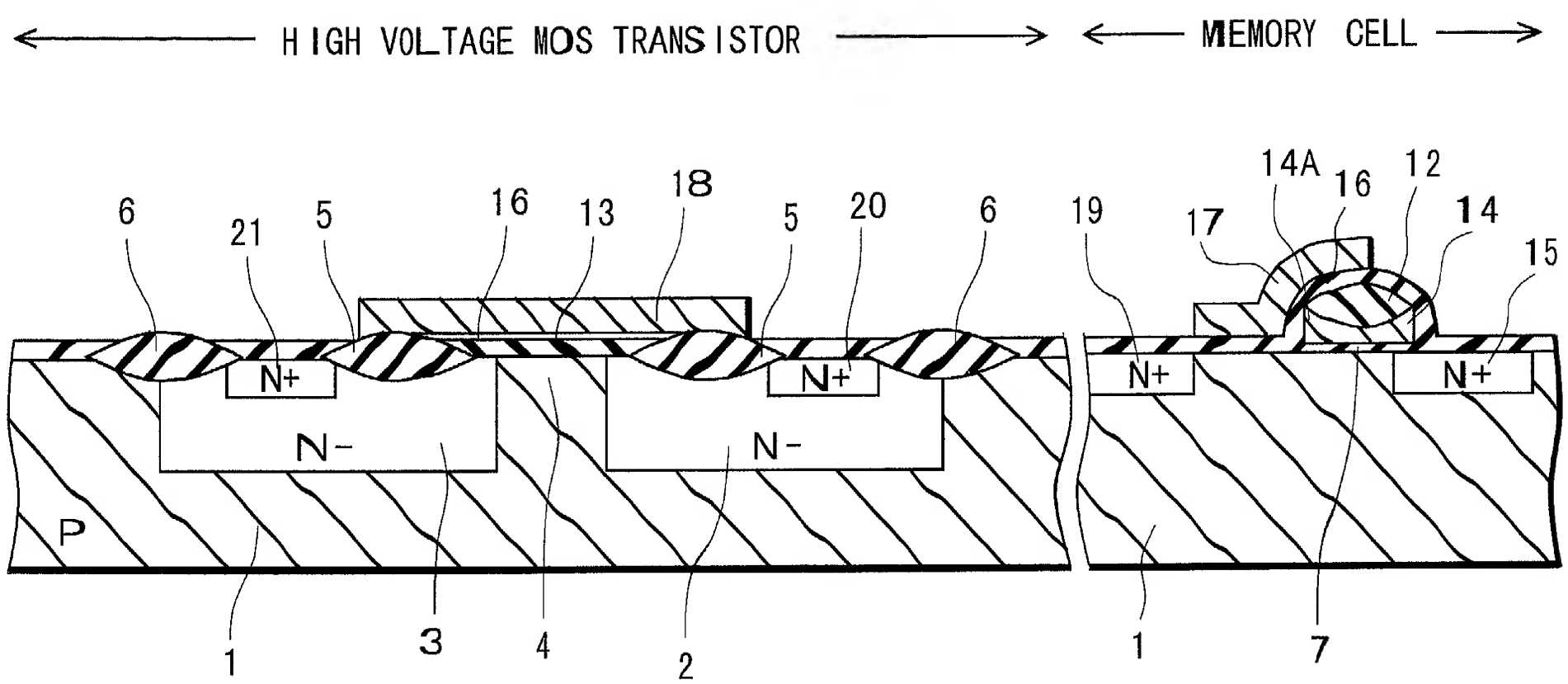
HIGH VOLTAGE MOS TRANSISTOR
MEMORY CELL
6
21
5
16
13
18
5
20
6
19
17
14A
16
12
14
15
N+
N+
N+
N+
N-
N-
P
1
3
4
2
1
7

FIG.7

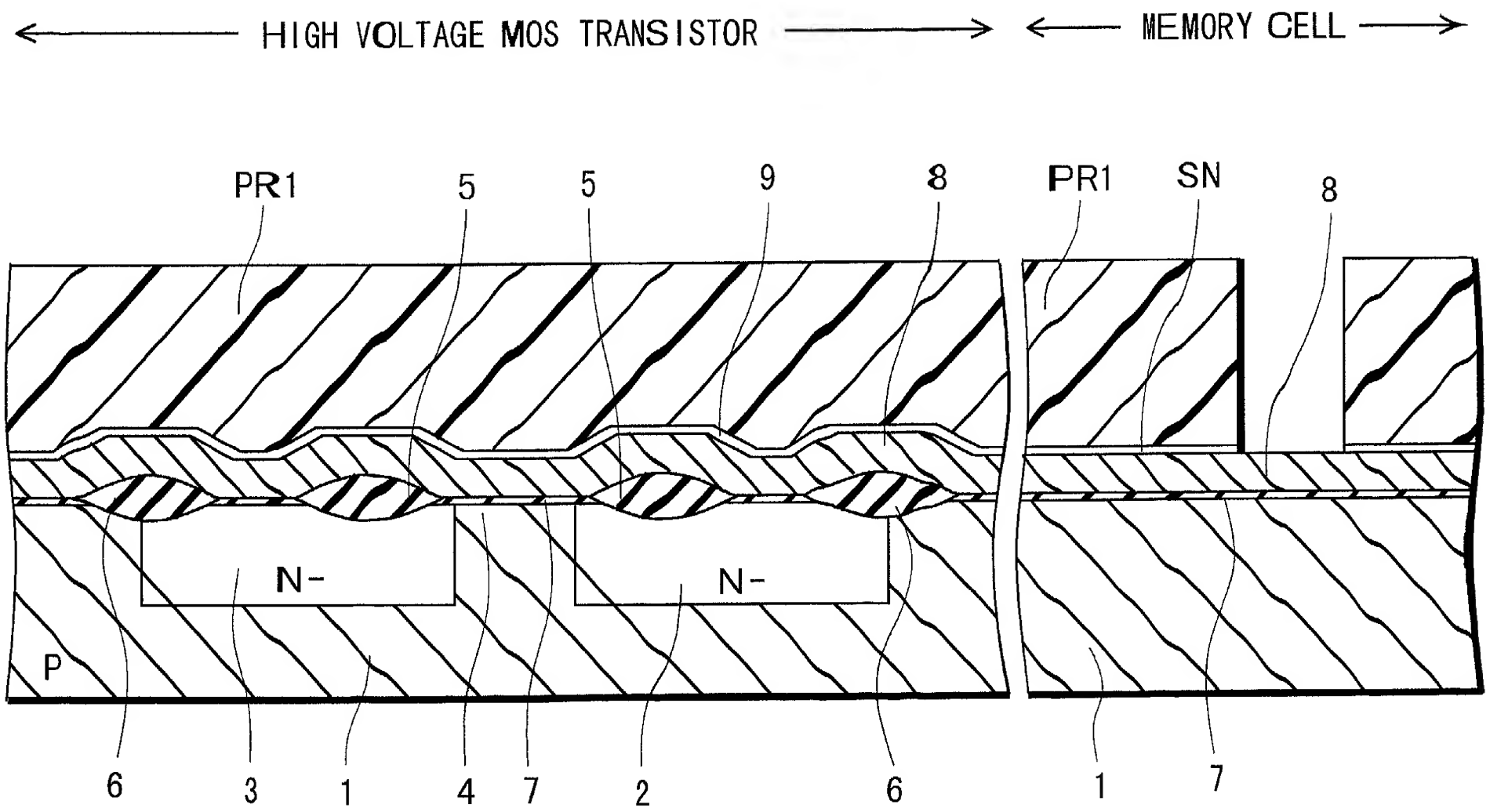
HIGH VOLTAGE MOS TRANSISTOR
MEMORY CELL
PR1
5
5
9
8
PR1
SN
8
N-
N-
P
6
3
1
4
7
2
6
1
7

FIG.8

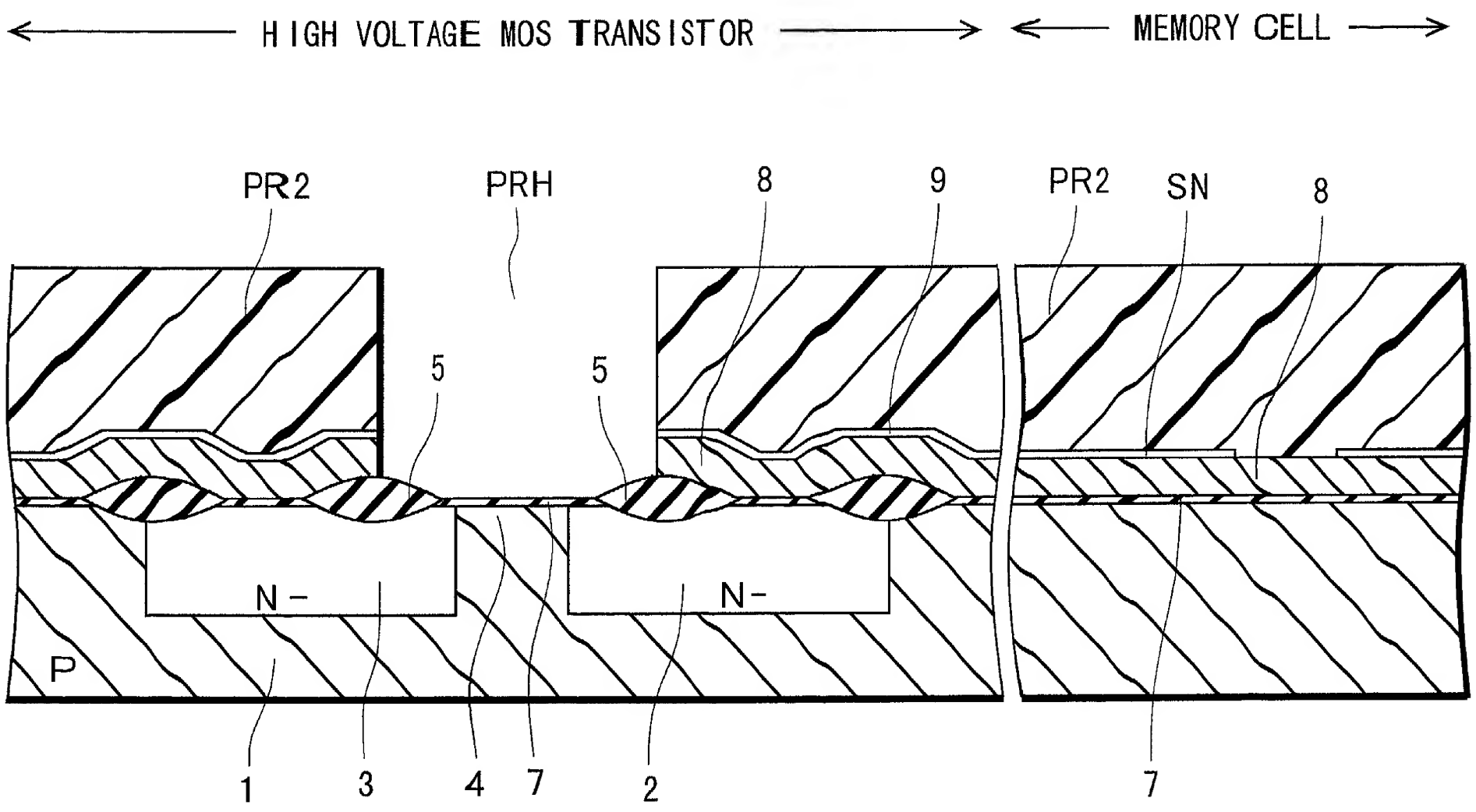
HIGH VOLTAGE MOS TRANSISTOR
MEMORY CELL
PR2
PRH
8
9
PR2
SN
8
5
5
N-
N-
P
1
3
4
7
2
7

FIG.9

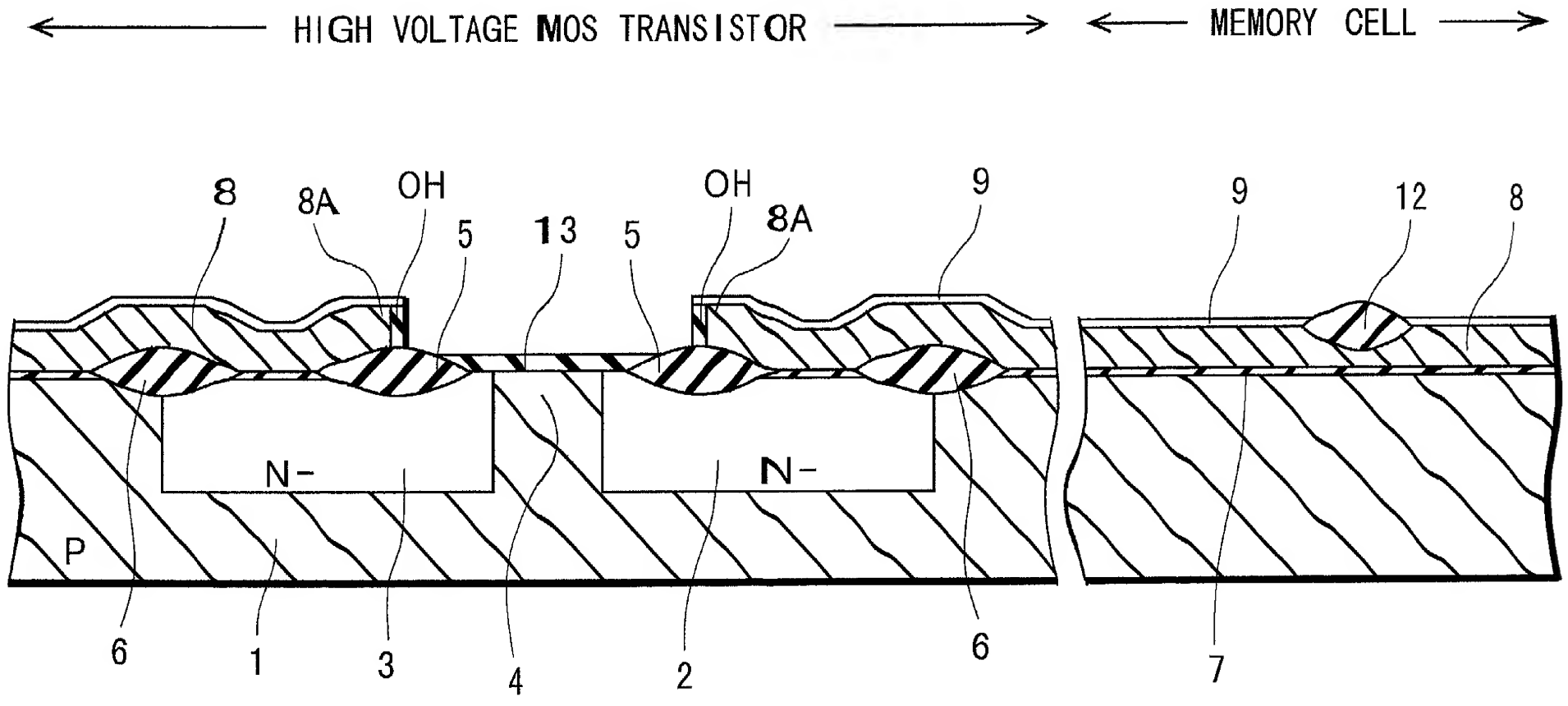
HIGH VOLTAGE MOS TRANSISTOR
MEMORY CELL
8
8A
OH
5
13
5
OH
8A
9
9
12
8
N-
N-
P
6
1
3
4
2
6
7

FIG.10

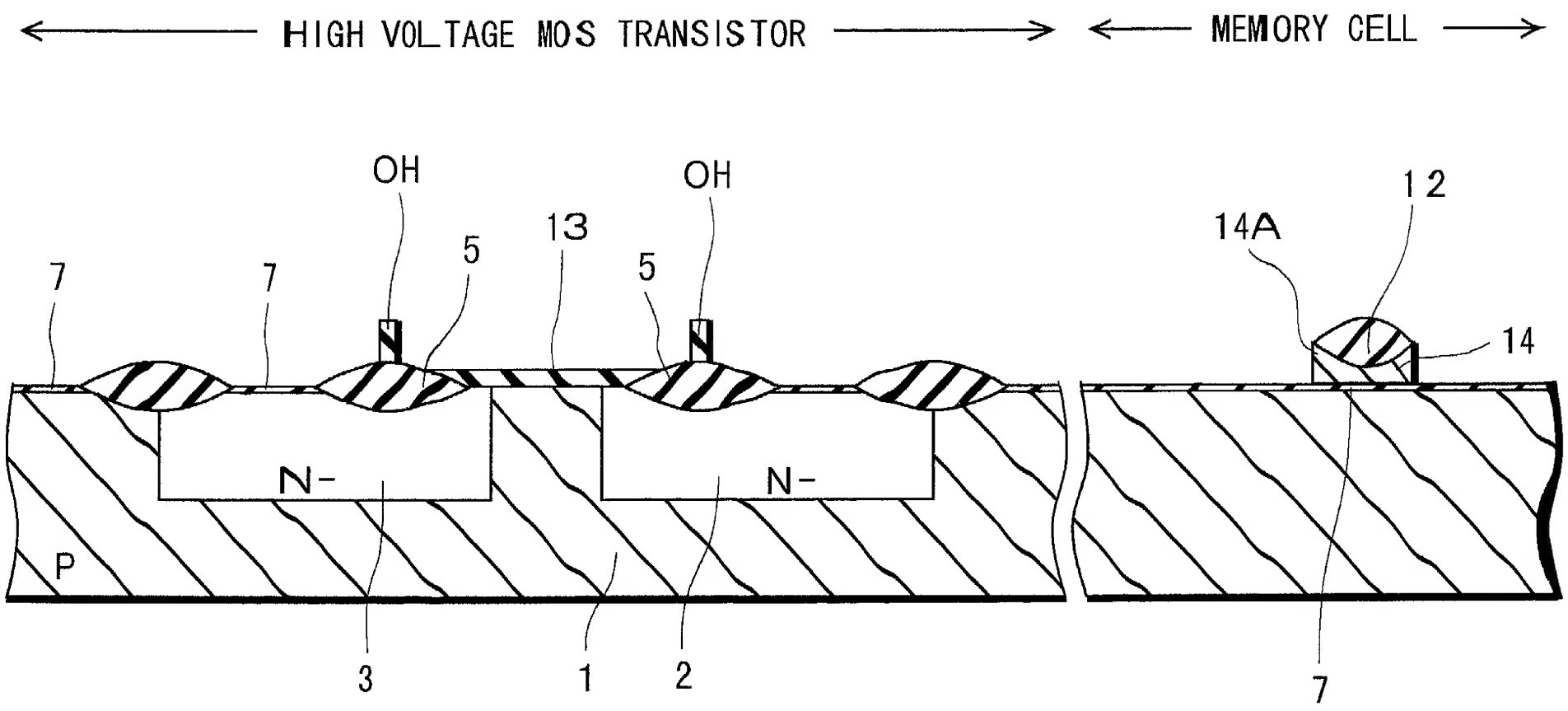
HIGH VOLTAGE MOS TRANSISTOR
MEMORY CELL
OH
OH
12
14A
13
5
5
14
7
7
N-
N-
P
3
1
2
7

FIG.11

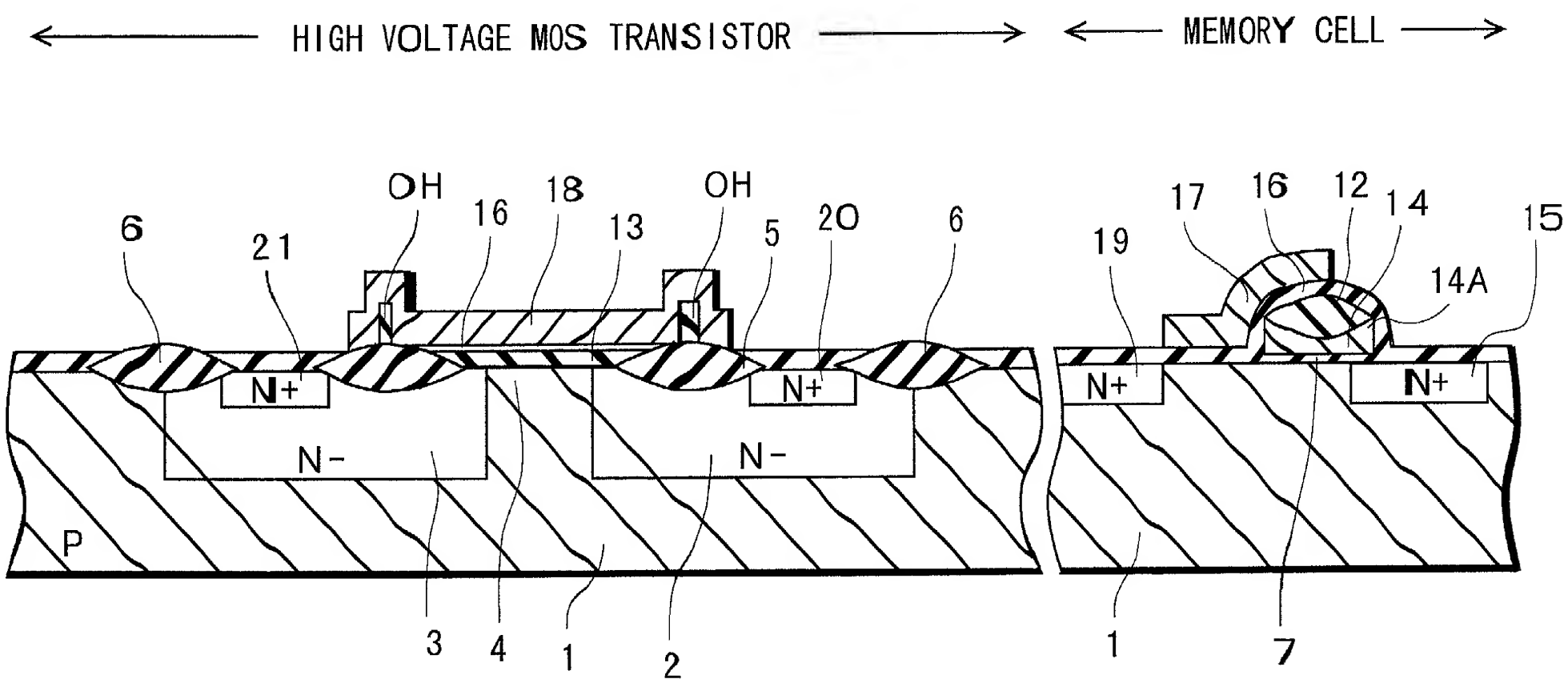
HIGH VOLTAGE MOS TRANSISTOR
MEMORY CELL
6
21
OH
16
18
13
OH
5
20
6
19
17
16
12
14
14A
15
N+
N+
N+
N+
N-
N-
P
3
4
1
2
1
7

FIG.12

PRIOR ART